WHAT IS CLAIMED IS:

1. A semiconductor package seal ring, comprising:

a plurality of insulating layers;

a plurality of conductive runners each embedded in one of the insulating layers, wherein each of the conductive runners includes an opening therein; and

a plurality of conductive posts each contacting one of the conductive runners and extending through at least one of the insulating layers and at least partially through the opening of another one of the conductive runners.

2. The semiconductor package seal ring recited in Claim 1 wherein each of the conductive posts is laterally disposed from other vertically adjacent conductive posts.

3. The semiconductor package seal ring recited in Claim 2 wherein a first half of the conductive posts are vertically aligned in a first column and a second half of the conductive posts are vertically aligned in a second column.

4. The semiconductor package seal ring recited in Claim 1 wherein the conductive runners comprise one selected from the group consisting of:

aluminum;

copper; and

doped silicon.

5. The semiconductor package seal ring recited in Claim 1 wherein the conductive posts comprise one selected from the group consisting of:

aluminum;

copper;

tungsten; and

doped silicon.

6. The semiconductor package seal ring recited in Claim 1 further comprising a plurality of films each interposing above one of the insulating layers and below one of the conductive runners.

7. The semiconductor package seal ring recited in Claim 6 wherein each of the films directly contacts an adjacent one of the insulating layers and an adjacent one of the conductive runners.

8. The semiconductor package seal ring recited in Claim 6 wherein the films are cap layers.

9. The semiconductor package seal ring recited in Claim 6 wherein the films comprise SiN.

10. The semiconductor package seal ring recited in Claim 1 wherein at least one of the conductive posts is in a dual-damascene structure.

11. The semiconductor package seal ring recited in Claim 1 further comprising a plurality of etch stop layers each interposing below one of the insulating layers and above one of the conductive runners.

12. A method of manufacturing a semiconductor package seal ring, comprising:

forming a first insulating layer;

forming first conductive runners in the first insulating layer;

forming a second insulating layer over the first insulating layer and the first conductive runners;

forming a first conductive post contacting at least one of the first conductive runners and extending at least partially through the second insulating layer and between two of the first conductive runners;

forming second conductive runners in the second insulating layer;

forming a third insulating layer over the second insulating layer and the second conductive runners; and

forming a second conductive post contacting at least one of the second conductive runners and extending at least partially through the third insulating layer and between two of the second conductive runners.

13. The method recited in Claim 12 wherein the first and second conductive posts are laterally disposed.

14. The method recited in Claim 12 wherein the first and second conductive runners comprise one selected from the group consisting of:

aluminum;

copper; and

doped silicon.

15. The method recited in Claim 12 wherein the first and second conductive posts comprise one selected from the group consisting of:

aluminum;

copper;

tungsten; and

doped silicon.

16. The method recited in Claim 12 further comprising:

forming a first cap layer between the first conductive runners and the second insulating layer; and

forming a second cap layer between the second conductive runners and the third insulating layer.

17. The method recited in Claim 12 wherein at least one of the first and second conductive posts is in a dual-damascene structure.

18. The method recited in Claim 12 further comprising forming a first etch stop layer between the second insulating layer and the second conductive runners.

19. A semiconductor device, comprising:

active devices located in a central portion of a substrate; and

a seal ring located at the periphery of the substrate, the seal ring including

a plurality of insulating layers;

a plurality of conductive runners each embedded in one of the insulating layers, wherein each of the conductive runners includes an opening therein; and

a plurality of conductive posts each contacting one of the conductive runners and extending through at least one of the insulating layers and at least partially through the opening of another one of the conductive runners.

20. The semiconductor device recited in Claim 19 wherein each of the conductive posts is laterally disposed from other vertically adjacent conductive posts.

21. The semiconductor device recited in Claim 20 wherein a first half of the conductive posts are vertically aligned in a first column and a second half of the conductive posts are vertically aligned in a second column.

22. The semiconductor device recited in Claim 19 wherein the conductive runners comprise aluminum.

23. The semiconductor device recited in Claim 19 wherein the conductive posts comprise tungsten.

24. The semiconductor device recited in Claim 19 wherein the seal ring further includes a plurality of cap layers each interposing above one of the insulating layers and below one of the conductive runners.

25. The semiconductor device recited in Claim 19 wherein at least one of the conductive posts is in a dual-damascene structure.

26. The semiconductor device recited in Claim 19 wherein the seal ring further includes a plurality of etch stop layers each interposing below one of the insulating layers and above one of the conductive runners.

27. A semiconductor package, comprising:

a substrate;

a plurality of insulating layers located over the substrate;

a plurality of conductive runners each located in one of the insulating layers over a periphery of the substrate, the conductive runners defining a plurality of columnar regions in the insulating layers that are unobstructed by the conductive runners; and

a plurality of conductive posts interconnecting the conductive runners, wherein each of the conductive posts is laterally offset from another vertically adjacent conductive post.

28. The semiconductor package recited in Claim 27 wherein the columnar regions include first and second columnar regions, wherein each of odd-numbered ones of the insulating layers includes a first one of the conductive posts located in the first columnar regions and not in the second columnar regions, and wherein each of even-numbered ones of the insulating layers includes a second one of the conductive posts located in the second columnar regions and not in the first columnar regions.